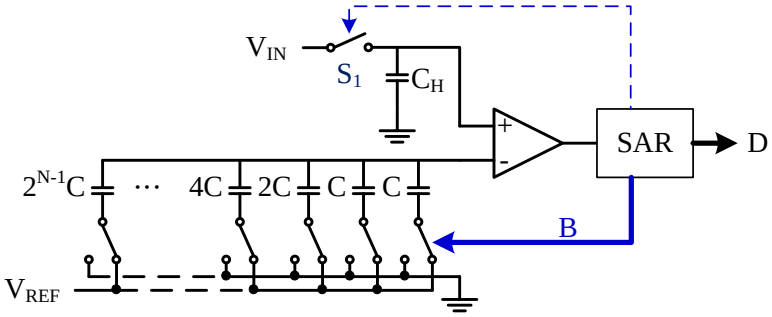
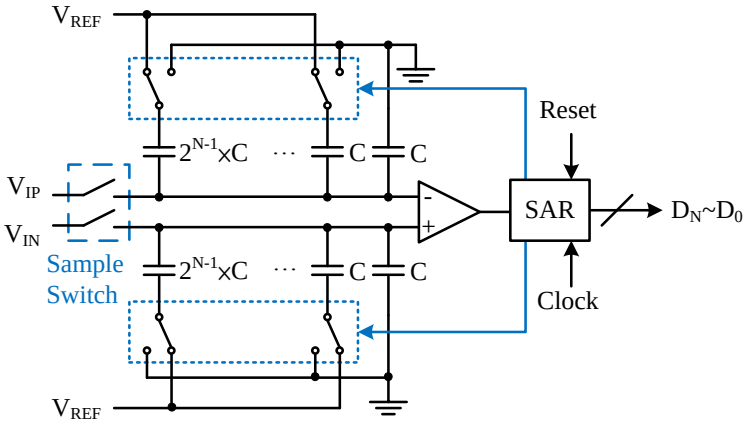
Successive-Approximation Analog-to-Digital Converter for Low-Power System Applications

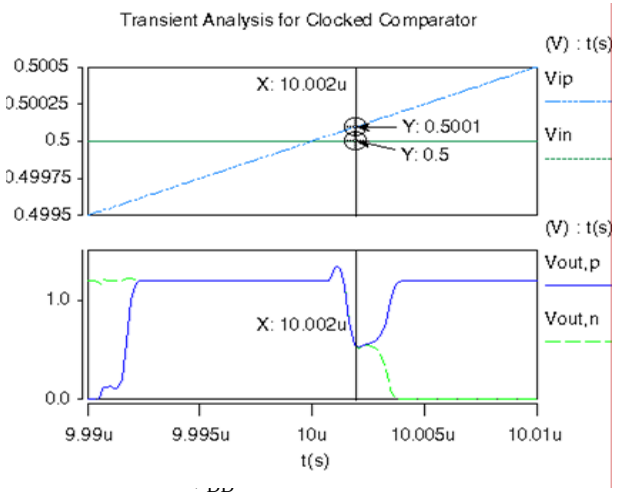
	Number of Comparator	Number of OPA[e]
Sigma-Delta[a]	1	1
Pipeline[b]	$2^k \times M$	$2 \times M$
Cyclic[c]	2^k	1
Successive Approximation	**1**	**0**
Flash	2^N	0
Time-interleaved[d]	$2^N \times P$	0

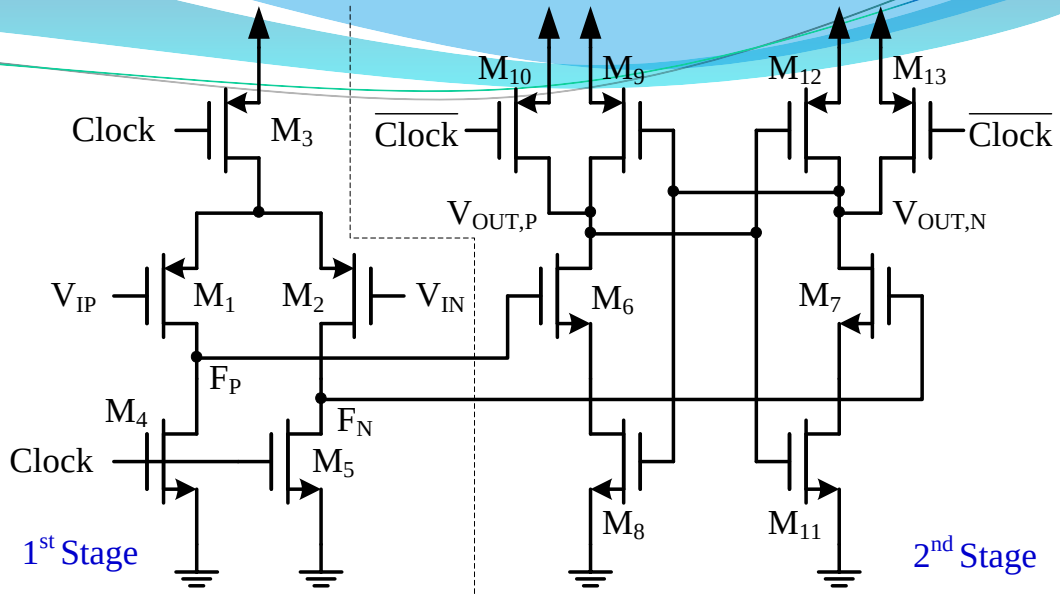
Note a: 1-bit Sub-ADC; b: k-bit Sub-ADC and M Stages;
c: k-bit Sub-ADC;
d: Architecture of Sub-ADC is Flash ADC and P Paths;
e: OPA is Operational Amplifier

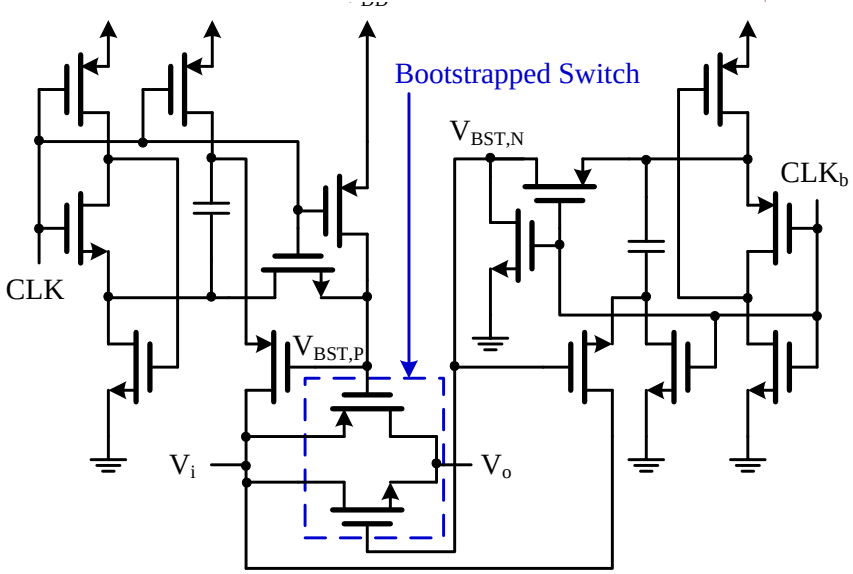


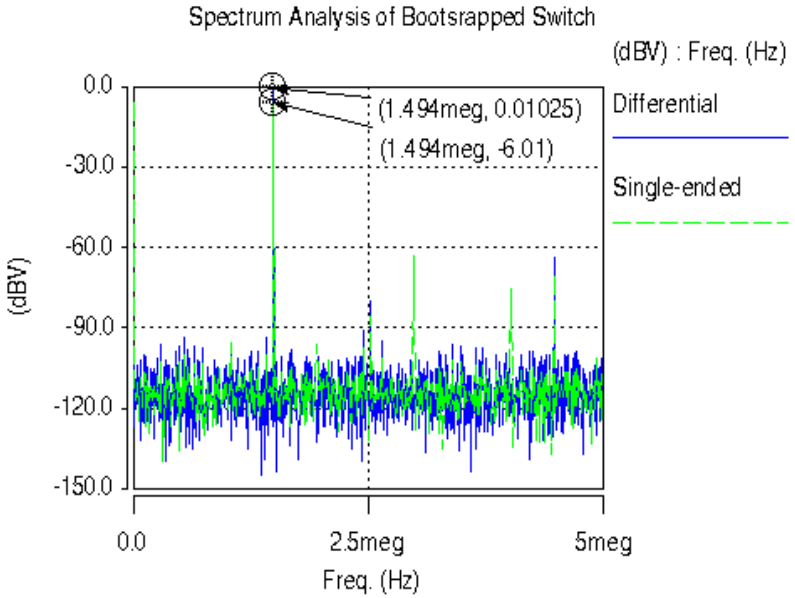


Sub-Circuits

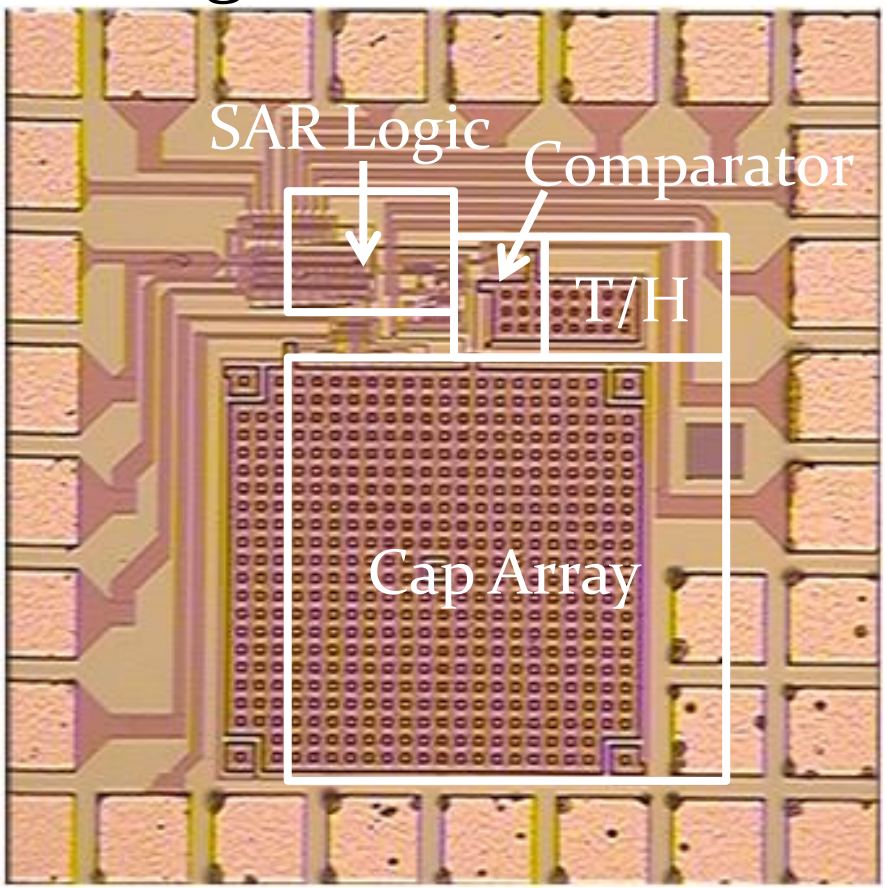








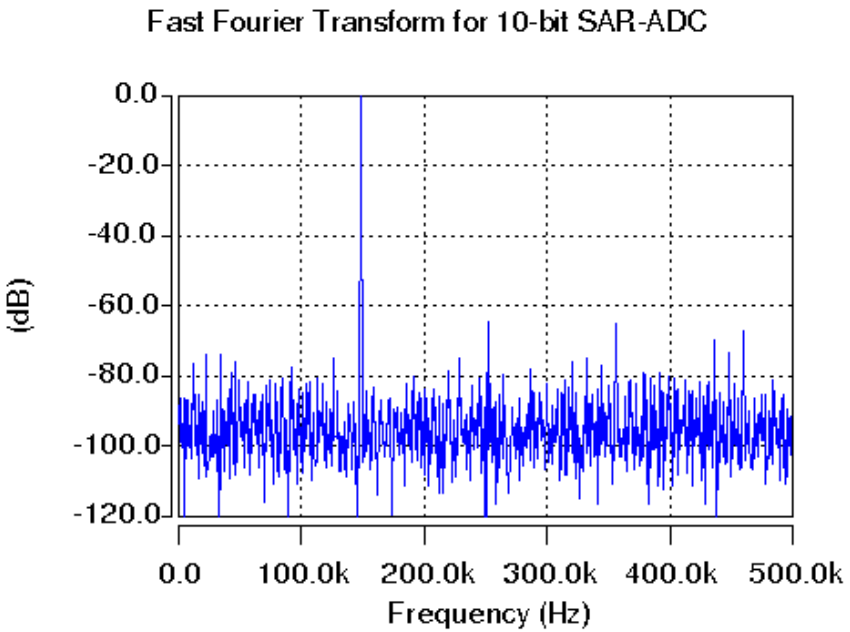
Single-Ended 1MS/s SAR-ADC



	Single-Ended
Supply Voltage (V)	1.8
Sample Rate (MS/s)	1
DNL (LSBs)	-0.37~0.51
INL (LSBs)	-0.37~0.31
SNR (dB)	47.690
SNDR (dB)	46.219
SFDR (dB)	57.718
ENOB	7.385
Power (Analog)	261.2 μW
Power (Digital)	12.1 μW
FoM (pJ/Conv.)	1.88
Area (including PAD)	780μm×780μm

$$FoM = \frac{Power}{2^{ENOB} \times f_s}$$

Fully-Differential 10-bitSAR-ADC



Sample Rate	1MS/s	10MS/s
INL (LSBs)	-2.1~2.1	-3.7~3.12
DNL (LSBs)	-1~2.2	-1.01~2.77
SNR (dB)	58.12	59.721
SNDR (dB)	57.02	54.734
SFDR (dB)	63.63	56.73
ENOB (bits)	9.17	8.8
Power (Analog)	15.3μW	187μW
Power (Digital)	6.6μW	76μW
FoM(fJ/Conv.)	38	59