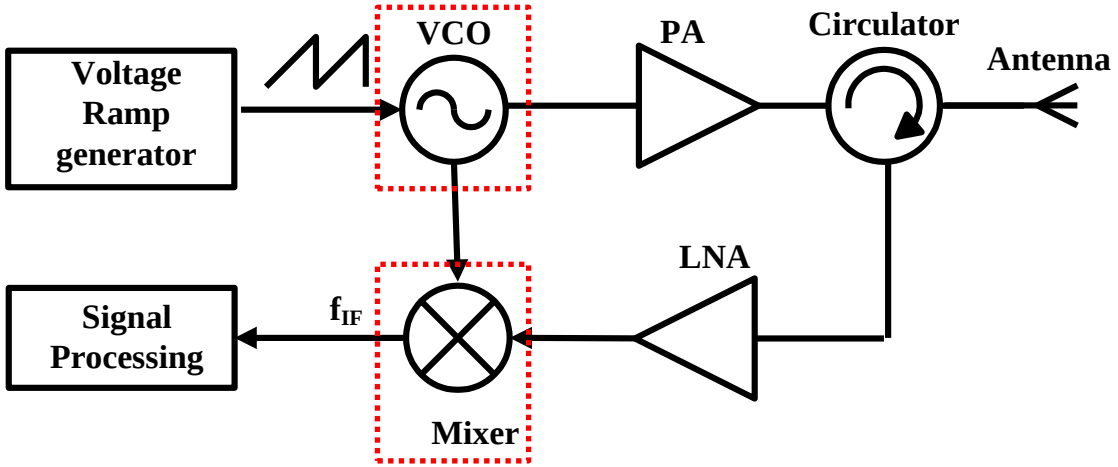
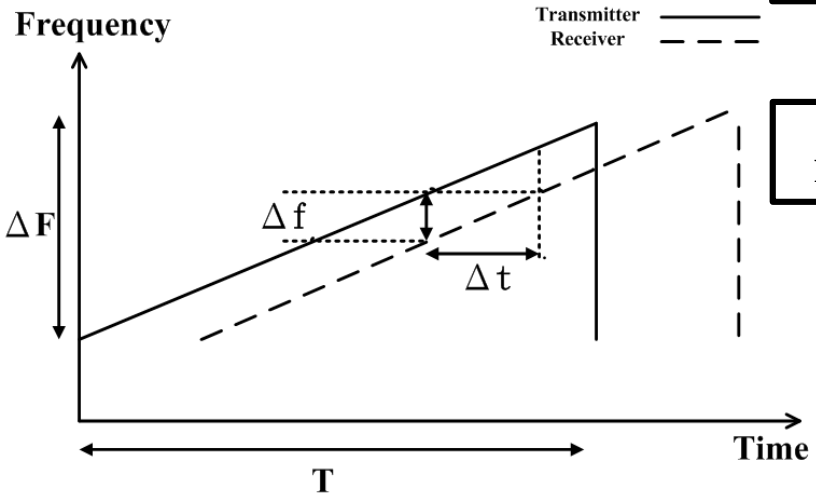
余紹萍(102級)

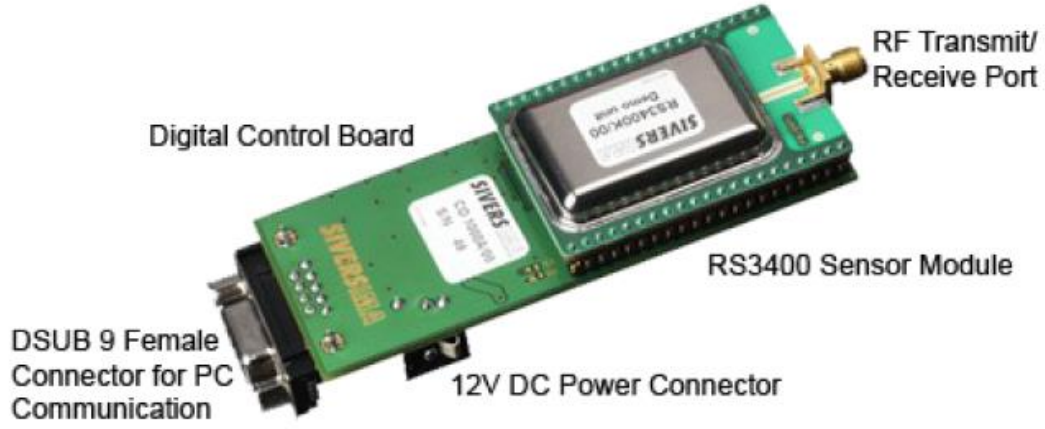
Circuit Design of Low-Power Voltage-Controlled Oscillator and Down-Conversion Mixer for 24 GHz Radar Systems

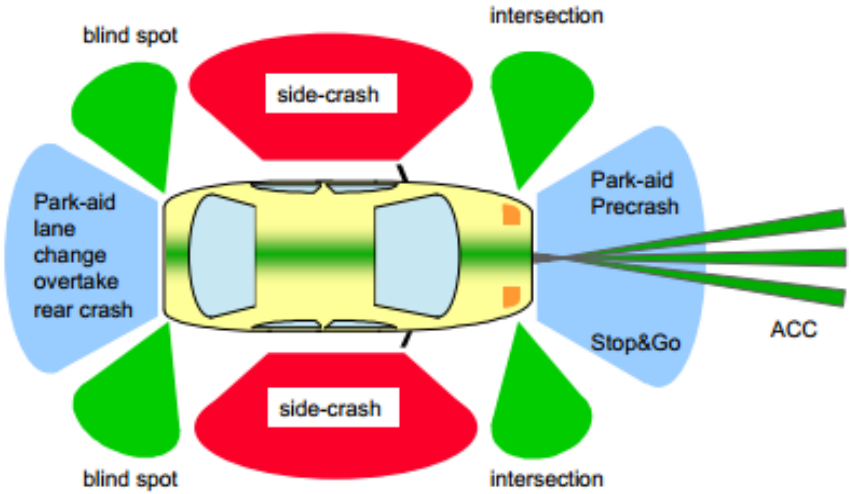
$$\Delta f = \frac{\Delta F}{T} \cdot \Delta t \qquad \Delta t = \frac{2R}{c}$$



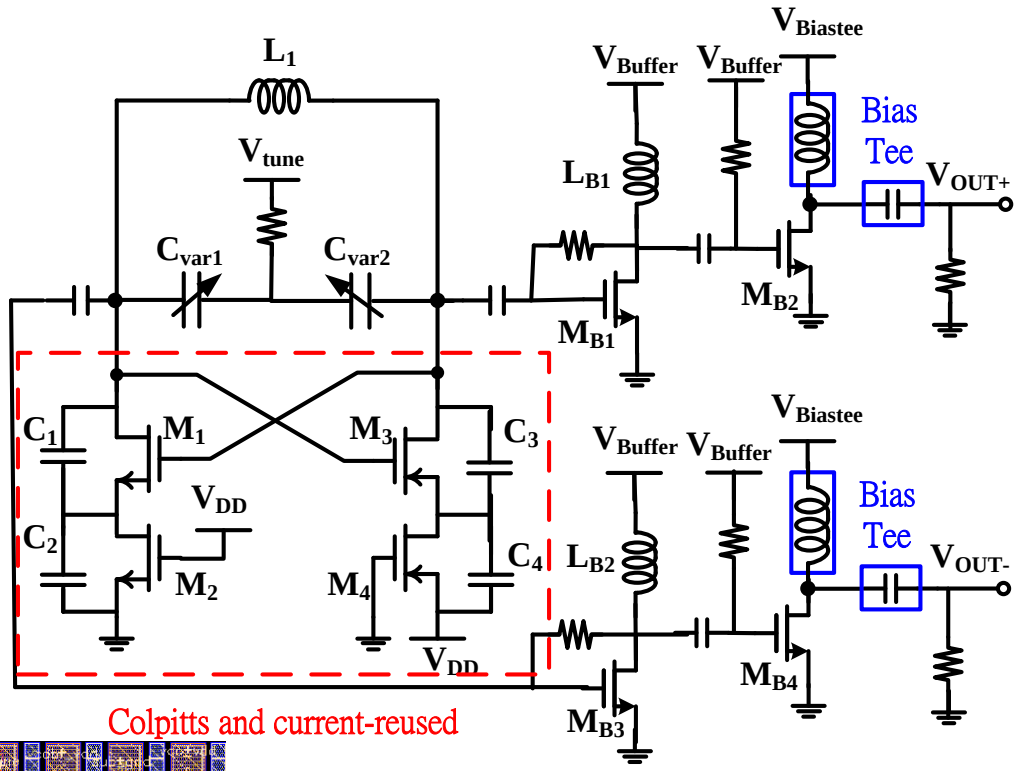


- The challenges of radar at 24 GHz
  - High cost
  - High power consumption

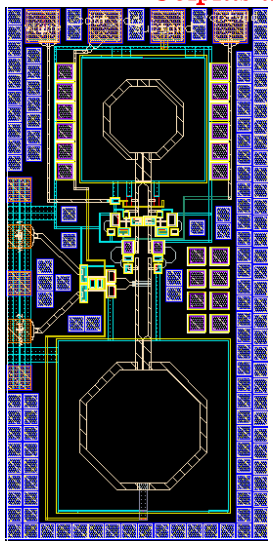




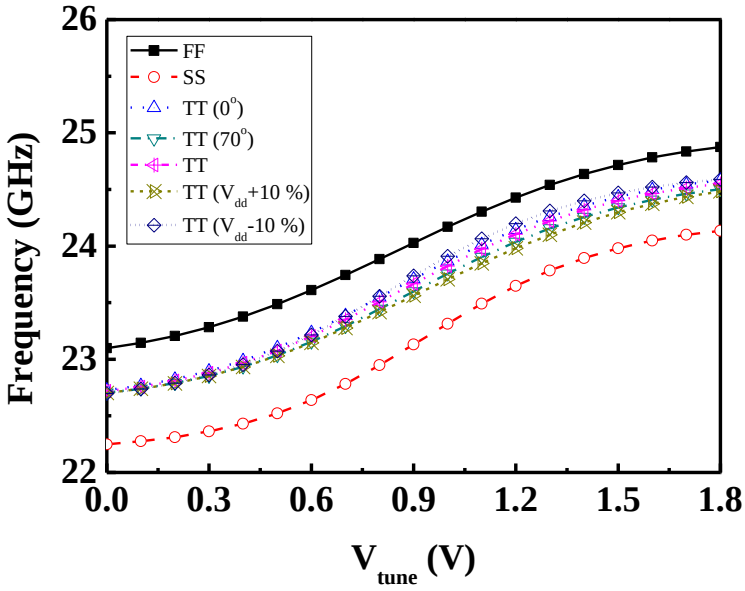
Design of Low-power VCO for 24 GHz Radar System

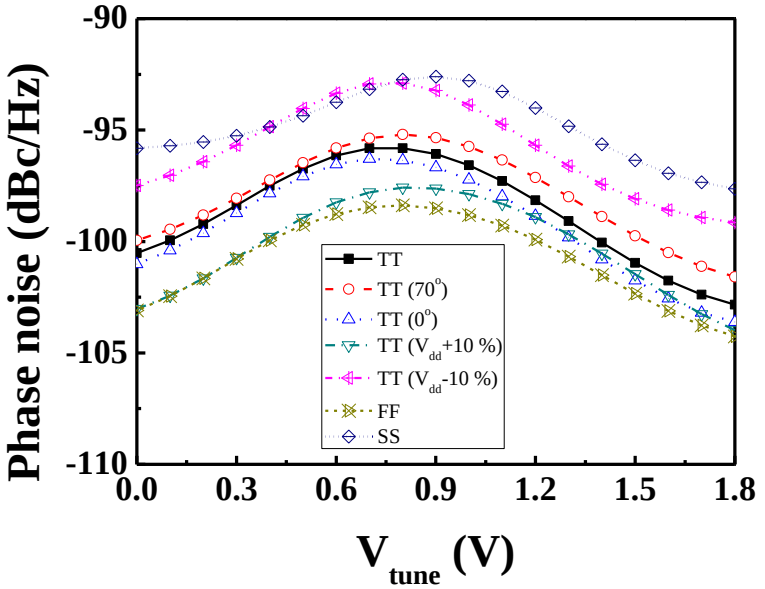


Colpitts and current-reused

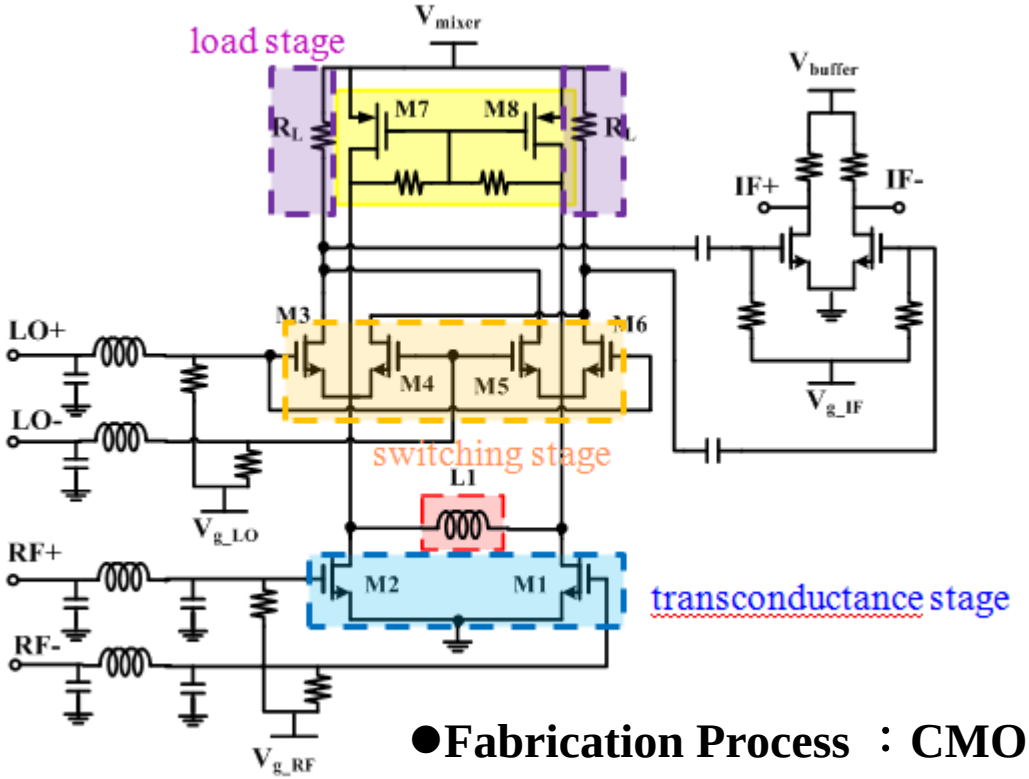


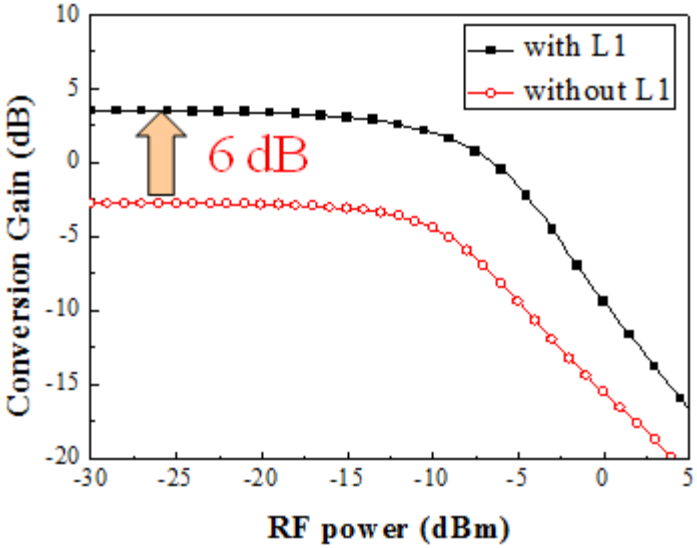
- Fabrication Process ： CMOS 0.18 μm
- Topology ： Current-reused+ Colpitts
- Tuning Range：22.72 ~ 24.55 (GHz)
- Core P_{DC}：3 (mW)
- Phase Noise@1 MHz：-102.8 (dBc/Hz)
- Phase Noise@10 MHz：-124 (dBc/Hz)
- FOM：-185.8 (dBc/Hz)
- Chip size：0.62 mm^2

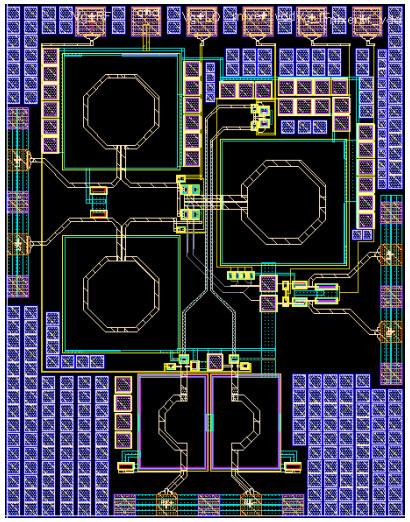




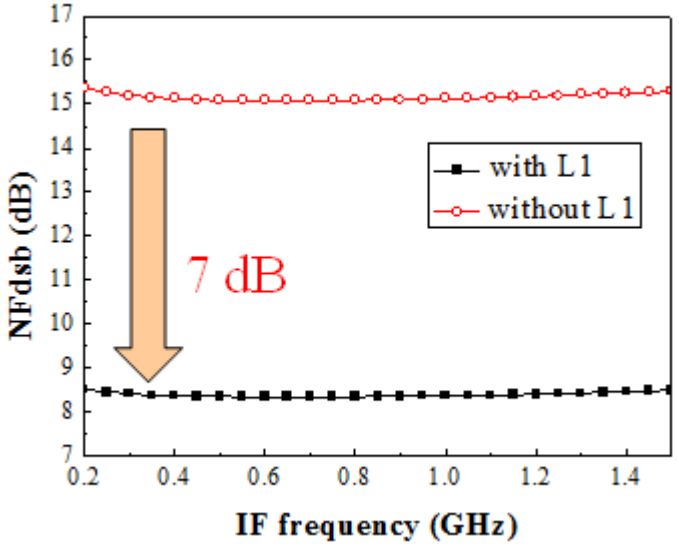
Design of Low-Power Gilbert-cell Mixer for 24 GHz Radar System



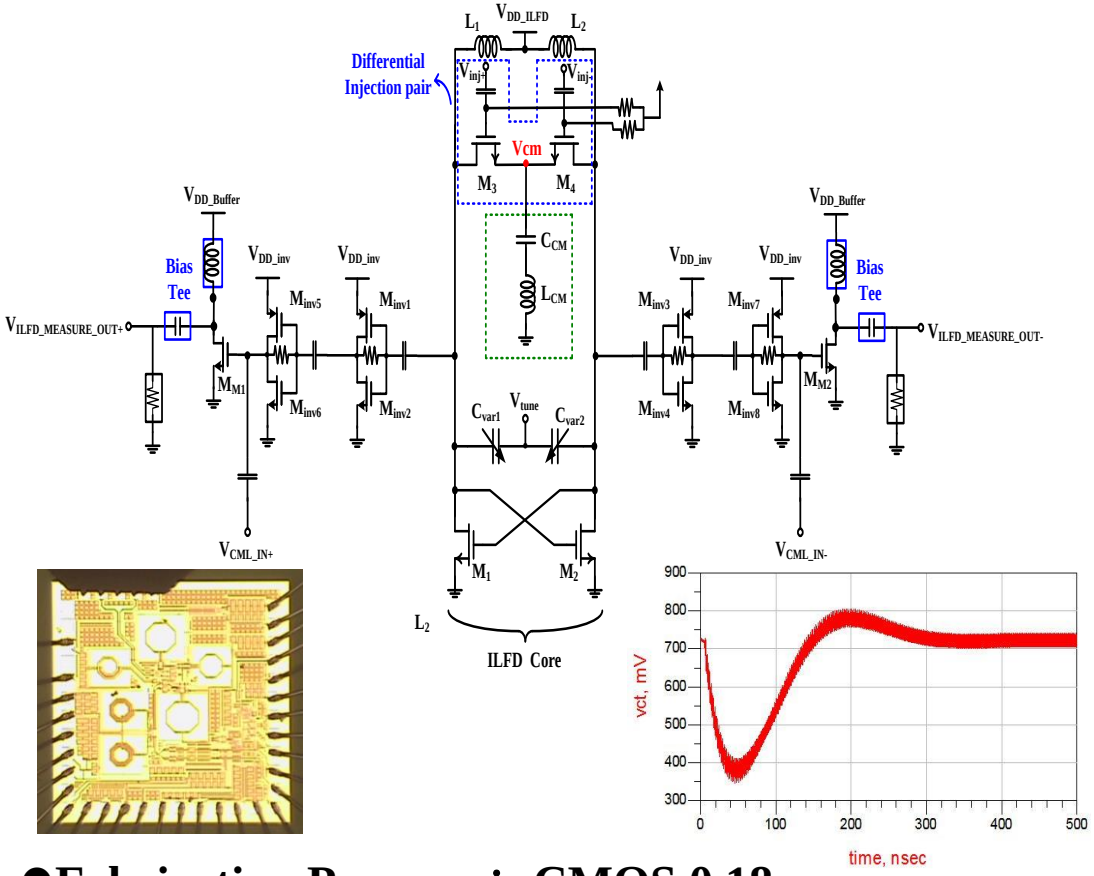


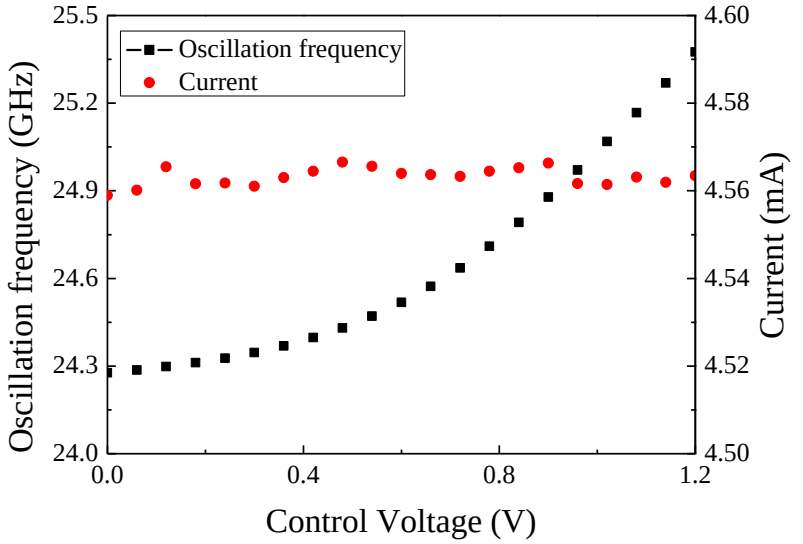


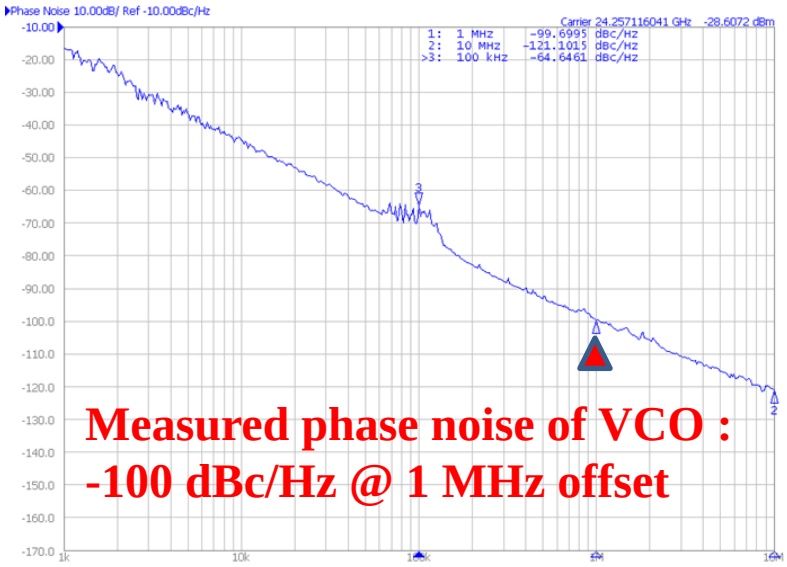
- **Fabrication Process ：CMOS 0.18 μm**
- **Topology ： Gilbert-cell**
- **Conversion Gain：3.5 (dB)**
- **Core P_{DC}：4.8 (mW)**
- **Noise figure ：8.5 (dB)**
- **Input P1dB：-11.5 (dBm)**
- **IIP3：-5 (dBm)**
- **Isolation：>44 (dB)**
- **FOM：10.686**
- **Chip size：1.14 mm^2**



Design of 24 GHz Phase-Locked Loop Using Divide-by-5 Prescaler







Measured phase noise of VCO : -100 dBc/Hz @ 1 MHz offset

- **Fabrication Process ： CMOS 0.18 µm**
- **Topology ： ILFD(/5)+CML(/2)+TSPC(/3 & /2)**
- **VCO Tuning Range：24.3 ~ 25.4 (GHz) (meas.)**
- **VCO Phase Noise@1 MHz：-100 (dBc/Hz) (meas.)**
- **VCO Phase Noise@10 MHz：-121 (dBc/Hz) (meas.)**
- **Total P_{DC}：40.85 (mW)**
- **Locking time : 400 (ns)**
- **PLL Chip size：1.72 mm^2**