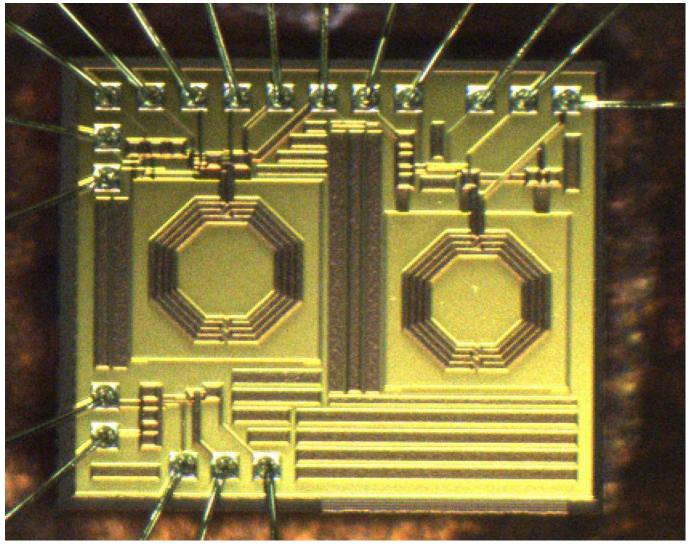

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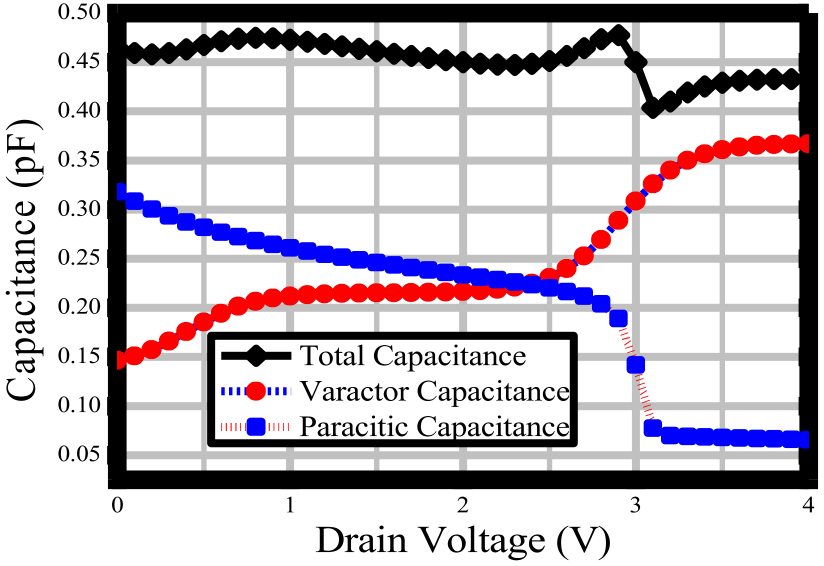

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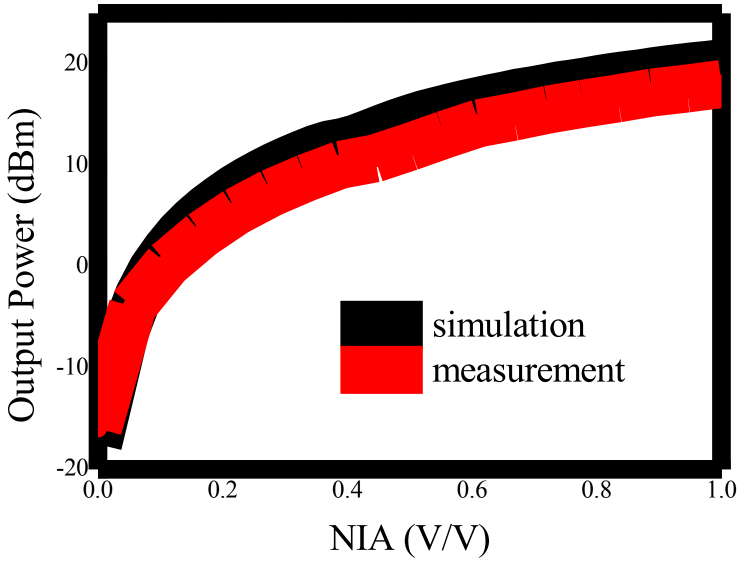

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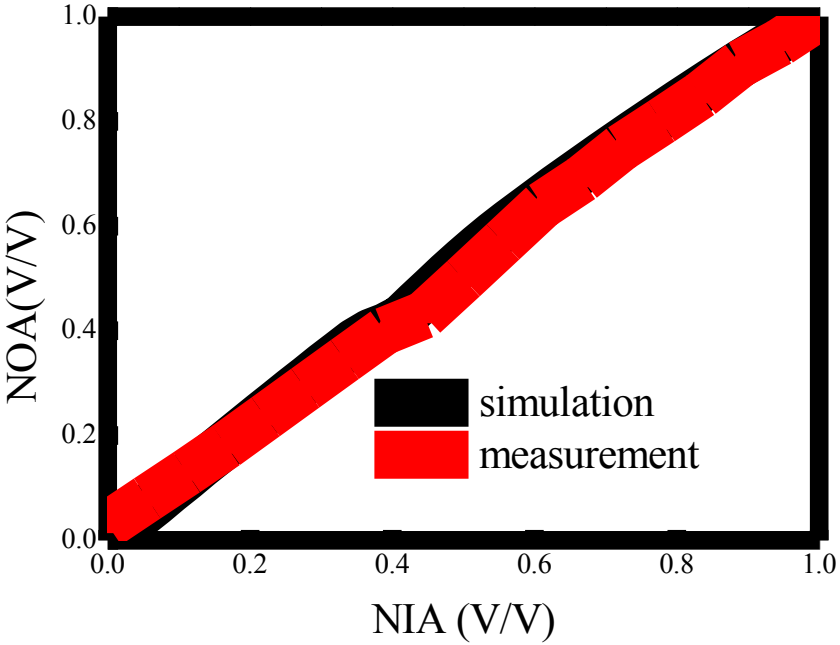

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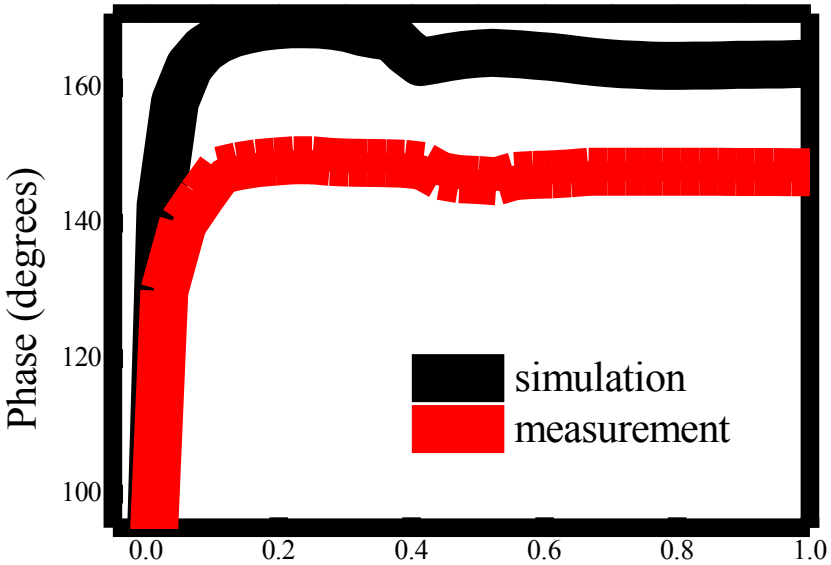

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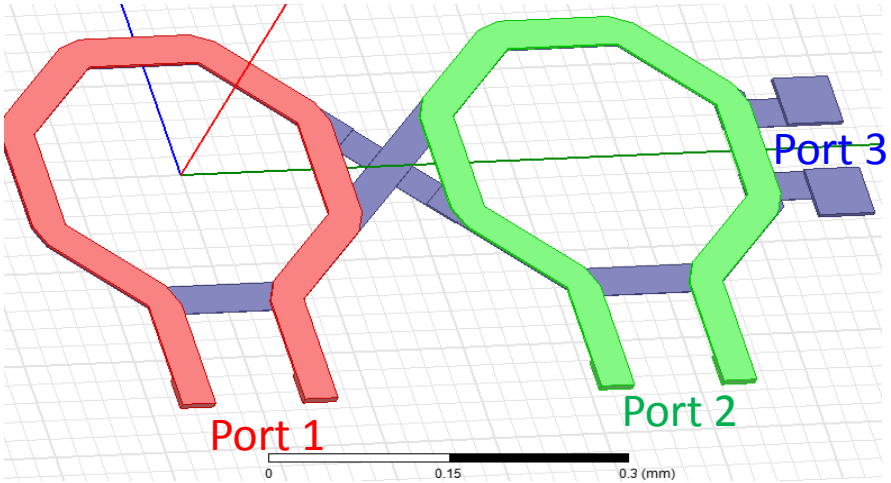
Parameter	[9]	[10]	This work
	APCCAS	JSSC	
Year	2009	2011	2012
Process (CMOS)	0.18	90	0.18
Frequency (GHz)	2.6	2.25	2.4
Pout (dBm)	16	25.2	18.03
DE (%)	36	-	43.7
PAE (%)	-	45	40.04
Vdd/PM (degrees)	3	37.5	3.1
Area (mm2)	2.16	1.04	1.198
Circuit	Auto Biasing	Switched Capacitor	Capacitance Compensation



“Figure 8” □□□□□□

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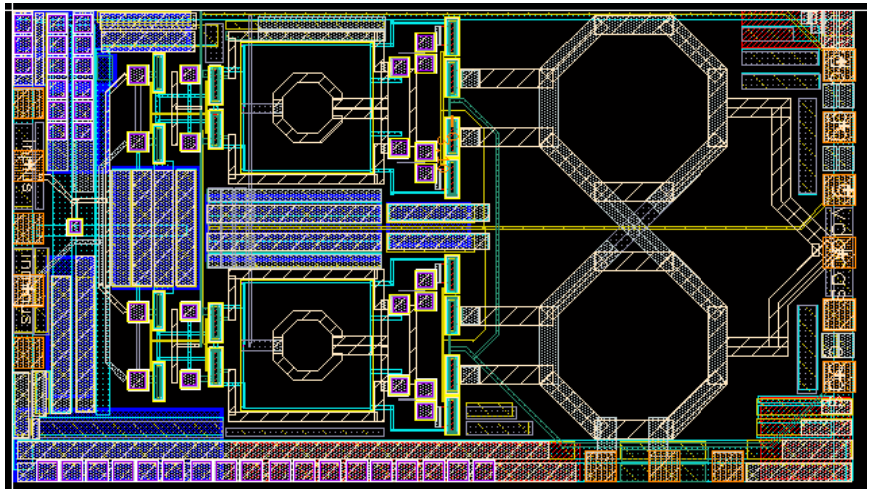

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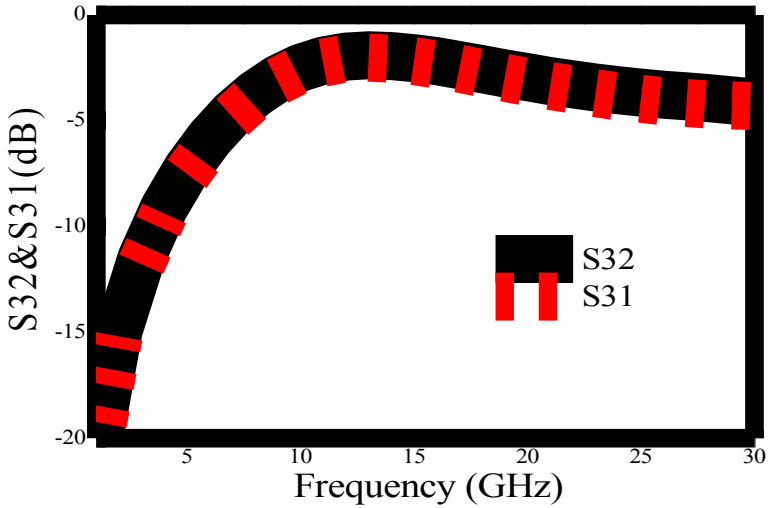

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- S32 is -3.56 dB, eff.=87 %
- S31 is -3.85 dB, eff.=82 %

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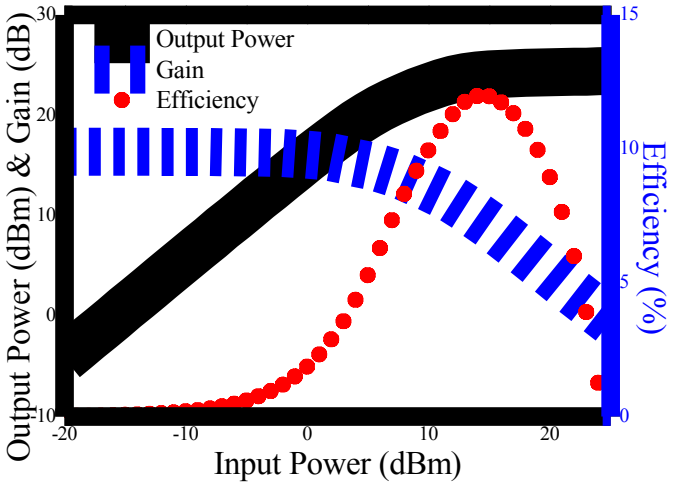
Ref.	[13]	[14]	[15]	This work
From	IMS	IET-CDS	MWCL	Post sim
Year	2011	2010	2009	2013
Process	0.18 μm CMOS			
Freq. (GHz)	22	23.5	22	24
Psat (dBm)	17.4	17.5	16.8	22.83
P1dB (dBm)	15.4	-	14.3	19.23
Gain (dB)	11.9	17.3	16.3	16.37
PAE (%)	12	8.8	10.7	11.14
FOM	45	146	106	529
Area (mm2)	0.4	1.98	0.35	1.01
Power Density (W/mm2)	0.1375	0.028	0.137	0.19
Circuit Description	Cascode 2 Stages Adaptive Bias	4 Combining CS 3 Stages Current Reuse	2 Combining Cascode 2 Stages	Transformer 2 Combining 3 Stages Cascode Differential

$$FOM = P_{OUT} \times Gain \times PAE \times f^2$$



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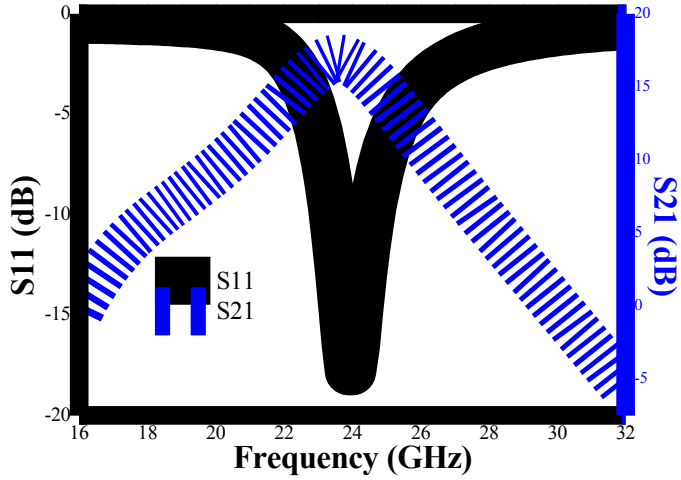

S11 □ S22